What is claimed is:

1. An alignment mark for use in a wafer alignment, comprising:

a first mark formed on a semiconductor layer;

a second mark formed adjacent to the first mark on the semiconductor layer; and

a concave part formed between the first mark and the second mark by etching a partial portion of the semiconductor layer,

wherein the alignment mark is used to align a wafer by detecting a zeroth order diffract light reflected from a sloped surface formed because of a difference in height between the concave part and the first or second mark.

2. The alignment mark for use in the wafer alignment as recited in claim 1, wherein a ± first order diffract light, a ± third order diffract light and ± fifth order diffract light each reflected from a flat upper surface of the first mark or the second mark are detected to be used for the wafer alignment.

3. The alignment mark for use in the wafer alignment as recited in claim 1, wherein the alignment mark is applicable for use in a laser scanning alignment (LSA) method, a field image alignment (FIA) method and a scribeline primary marks (SPM) method.

4. The alignment mark for use in the wafer alignment as recited in claim 2, wherein the alignment mark is applicable for use in a laser scanning alignment (LSA) method, a field image alignment (FIA) method and a scribeline primary marks (SPM) method.

5. A method for fabricating an alignment mark for use in a wafer alignment, comprising the steps of:

etching selectively a semiconductor layer by using a first mask pattern to form a plurality of concave parts with a predetermined consistent distance on the semiconductor layer;

depositing a material on an entire surface of a structure containing the concave parts; and

etching selectively the deposited material by using a second mask pattern to form a first mark and a second mark.

6. The method as recited in claim 5, wherein the first mask pattern and the second mask pattern include a layout for forming an isolation pattern, a gate electrode pattern, a bit line pattern, a landing plug contact (LPC) pattern, a storage node contact (SNC) pattern, metal patterns (M1 and M2) and a metal contact (MC) pattern.

7. The method as recited in claim 5, wherein the alignment mark is applicable for use in a laser scanning alignment (LSA) method, a field image alignment (FIA)

method and a scribeline primary marks (SPM) method.